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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 042390.P6942 Total Pages 3

First Named Inventor or Application Identifier Mark D. Nardin

Express Mail Label No. EL371007742US

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APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. XX Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. XX Specification (Total Pages 22)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 8)

4. ____ Oath or Declaration (Total Pages ___)
   a. ___ Newly Executed (Original or Copy)
   b. ___ Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**
   i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ____ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ____ Microfiche Computer Program (Appendix)

7. _____ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)
_____ b. Power of Attorney
10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449
_____ b. Copies of IDS Citations
12. _____ Preliminary Amendment
13. __X__ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
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16. __X__ Other: Express Mail Certification
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Serial/Patent No.: **** Filing/Issue Date: Herewith

Client: Intel Corporation

Title: METHOD AND APPARATUS FOR FULLY AUTOMATED SIGNAL INTEGRITY ANALYSIS FOR DOMINO CIRCUITRY

BSTZ File No.: 042390.P6942 Atty/Secty Initials: GEV/bh

Date Mailed: 12-30-99 Docket Due Date: ****

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- ☐ Appeal Brief (____ pgs.) (in triplicate)
- ■ Application - Utility (22 pgs., with cover and abstract)
- ☐ Application - Rule 1.53(b) Continuation (____ pgs.)
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- ☐ Power of Attorney (____ pgs.)
- ☐ Preliminary Amendment (____ pgs.)
- ☐ Reply Brief (____ pgs.)
- ☐ Response to Notice of Missing Parts
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☐ Other: ____

UNITED STATES PATENT APPLICATION

FOR

METHOD AND APPARATUS FOR FULLY AUTOMATED SIGNAL INTEGRITY ANALYSIS FOR DOMINO CIRCUITRY

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Attorney's Docket No: 042390.P6942

METHOD AND APPARATUS FOR FULLY AUTOMATED SIGNAL INTEGRITY ANALYSIS FOR DOMINO CIRCUITRY

BACKGROUND OF THE INVENTION

Field of the Invention

This invention generally relates to design and simulation of integrated circuits and more specifically relates to simulation of domino logic circuits for use in integrated circuits.

Description of the Related Art

Domino circuitry is a well recognized branch of digital logic circuitry. However, due to its dynamic nature, it is inherently susceptible to noise in a way that static circuitry, the other well recognized branch of digital logic circuitry, is less susceptible. Domino circuitry tends to propagate noise, rather than damping out noise as static circuitry tends to. As a result, simulating domino circuitry to determine whether it is susceptible to noise either generated within the circuit or received from prior stages or surrounding circuitry is of great importance.

Integrated circuits utilizing domino circuitry are becoming more and more complex. Transistor minimum geometries are shrinking, the dies upon which these transistors exist are increasing in size, and therefore the number of circuits that can be placed on an integrated circuit is increasing. As a result of these increases more highly interconnected domino circuitry is included in each complex digital integrated circuit.

Furthermore, more opportunities exist for some form of crosstalk or other noise inducing phenomenon. Crosstalk typically occurs when two conductors are located close to each other physically. These two conductors are typically not actually connected or otherwise coupled together intentionally by a designer. However, some form of coupling occurs as a result of which a change of the voltage on a first conductor such as the transition from a high-to-low or low-to-high logic state will result in some form of noisy transition or change in logic state of a second conductor. This transition or change on the second conductor, which is not caused by whatever logic is driving the second conductor, results in noise which may be propagated through any domino circuitry coupled directly to the second conductor. Once propagated through that domino circuitry it may be propagated through further stages of domino circuitry. As a result it is of great importance that domino circuitry be simulated both in terms of its susceptibility to noise but also in terms of how the physical layout of the domino circuitry and its incoming and outgoing conductors tends to lead to noise being injected into the circuitry.

Classically, each stage of a circuit has been simulated independently, therefore a designer would have to design a simulation for each stage of his or her circuit and then in some manner determine what the worst-case results of preceding stages were in order to simulate the noise characteristics of whichever stage the designer is focusing on at that time. As circuits get more and more complicated and as designers are responsible for larger and larger portions of circuitry, this approach becomes inherently unwieldy, to the point where a designer may be expected to spend significantly more

time simulating the circuitry than could possibly be allowed for in today's rapid-paced and tight schedules.

SUMMARY OF THE INVENTION

In one embodiment, the invention is a method. The method includes extracting parameters of a set of domino logic circuits. The method also includes simulating each domino logic circuit of the set of domino logic circuits. Also, the method includes reporting results of the simulation.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures.

Figure 1A illustrates an example of how incorrect data may be latched independent of clock frequency.

Figure 1B illustrates waveforms corresponding to the signals on various conductors in the circuitry of Figure 1A.

Figure 2 illustrates an embodiment of a domino circuitry stage along with potential noisy input and output waveforms.

Figure 3 illustrates an overview schematic of multiple cascaded domino stages.

Figure 4A illustrates one embodiment of a method of simulating domino circuitry.

Figure 4B illustrates an alternate embodiment of a method of simulating domino circuitry.

Figure 5 illustrates one embodiment of a method of designing and simulating domino and other circuitry.

Figure 6 illustrates a machine readable medium embodying instructions suitable for use on a processor for causing the processor to execute the method of Figure 4.

Figure 7 illustrates a system suitable for implementing the method of Figure 4 or alternative embodiments of a method of simulating domino circuitry.

DETAILED DESCRIPTION

A method and apparatus for fully automated signal integrity analysis for domino circuitry is described. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the invention. It will be apparent, however, to one skilled in the art that the invention can be practiced without these specific details. In other instances, structures and devices are shown in block diagram form in order to avoid obscuring the invention.

Reference in the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. The appearances of the phrase "in one embodiment" in various places in the specification are not necessarily all referring to the same embodiment, nor are separate or alternative embodiments mutually exclusive of other embodiments.

Figure 1 illustrates an example of how incorrect data may be latched independent of clock frequency. A first conductor 110 is coupled to a first inverting stage 115. The first inverting stage 115 is coupled to a second conductor 120 which in turn is coupled to a second inverting stage 125. The second inverting stage 125 is coupled to a conductor 130 which in turn is coupled to the data input of a flip-flop or register 135. A fourth conductor 170 is coupled to the clock stage, the clock input of a second flip-flop or register 175. The output of flip-flop 175 is coupled to a fifth conductor 160. Conductor 160 is cross-coupled through a parasitic capacitance 150 to conductor 110. Conductor 170, aside from being coupled to flip-flop 175, is also coupled to third inverting stage 177. Third inverting stage 177 is coupled to a conductor

which is coupled to fourth inverting stage 178. Fourth inverting stage 178 is coupled to a conductor which is coupled to fifth inverting stage 179. Fifth inverting stage 179 is coupled to a conductor 180 which is coupled to the clock input of flip-flop 135. The output of flip-flop 135 is coupled to conductor 140. Conductor 110 has the signal A associated with it. Conductor 110 therefore conducts the signal A. Conductor 120 conducts the signal B. Conductor 130 conducts the signal C. Conductor 160 conducts the signal D. Conductor 170 conducts the signal CLK1. Conductor 180 conducts the signal CLK2 and conductor 140 conducts the signal OUT.

Turning to Figure 1B the waveforms for conductors CLK1 A, B, C, D, CLK2 and OUT are all illustrated. In particular the incorrect data latched by flip-flop 135 and propagated through conductor 140 as OUT as illustrated. Note that signal A rises due to its cross coupling on conductor 110 through a capacitance 150 to conductor 160 which carries signal D. Signal D was latched at flip-flop 175 as a result of the transition on CLK1. This transition on conductor 160 or signal D results in the partial transition of signal A. This is propagated as a full transition to signal B and likewise as a full transition to signal C. CLK2 is a delayed version of CLK1 and at the time CLK2 transitions at flip-flop 135, signal C is in its erroneous state and therefore the wrong data is latched on flip-flop 135 and propagated through signal OUT.

Turning to Figure 2, an embodiment of the single stage domino circuit is illustrated. MOSFET 215 is controlled at its gate electrode by CLK (Clock) 210. One node of MOSFET 215 is coupled to VCC 220. The other node of MOSFET 215 is coupled to a second node of MOSFET 285. A first leg of MOSFET 285 is likewise coupled to Vcc 220. The gate electrode of MOSFET 285 is coupled to the output of

inverting stage 275. The second leg of MOSFET 215 and the second leg of MOSFET 285 is coupled to the input of inverting stage 275. Input A is carried on conductor 230 which is coupled to the gate electrode of MOSFET 235. The first leg of MOSFET 285 is coupled to the second leg of MOSFET 215 and the second leg of MOSFET 285. A second leg of MOSFET 235 is coupled to a first a leg of MOSFET 245. The second leg of MOSFET 245 is coupled to ground. The gate electrode of MOSFET 245 is coupled to conductor 240 which carries the signal B. Conductor 250 carries the signal VDO and is coupled to the input of inverting buffer 275, the first leg of MOSFET 235, the second leg of MOSFET 215 and the second leg of MOSFET 285. Conductor 250 is coupled to the input of inverting output buffer 265. Furthermore conductor 250 is coupled to a parasitic capacitance 255, also labeled C_{xcap}, which is coupled to another conductor independent of this embodiment of the domino circuit stage. Also illustrated in Figure 2 are waveforms for signal A and signal B illustrating previously found worst-case noise waveforms for each of these two signals. Likewise a waveform for signal VDO, which is the output of this stage, is illustrated. This waveform is the waveform determined by simulation based on waveforms for signals A and B and it illustrates the worst-case output of this stage.

Turning to Figure 3, an overview schematic of a number of stages of domino circuitry is illustrated. Stage 305 is a domino nand gate. Stage 310 is a domino nor gate. The output of stage 305 is coupled to the first input of stage 315, a static nand gate. Likewise the output of stage 310 is coupled to the second input of stage 315. The output of stage 315 is coupled to a first input of stage 320, which is another domino nor gate. The output of stage 320 is coupled to the input of stage 325 which is a static

inverting buffer. The output of stage 325 is coupled to a first input of stage 330 which is a domino nand gate.

Stage 340 is a domino nand gate. The output of stage 340 is coupled to the first input of stage 350 which is a static nand gate. Stage 345 is a domino nor gate and the output of stage 345 is coupled to a second input of stage 350. The output of stage 350 is coupled to the input of inverting buffer 355 which is a static circuit. The output of stage 355 is coupled to a first input of stage 360 which is a nand gate and is also a static circuit. The output of stage 360 is coupled to a second input of stage 330 and is also coupled to a first input of stage 365 which is a domino nand gate. The output of stage 330 is coupled to the first input of stage 375 which is a static nand gate. The output of stage 365 is coupled to a second input of stage 375. Circuits 305, 310, 320 and 330 are all domino circuits and represent cascaded stages of domino circuitry (with some static circuitry intervening. Circuits 340, 345 and 365 are also domino circuits. It will be appreciated that the circuitry illustrated in Figure 2 is one embodiment of circuitry suitable for implementing domino nor gate 320 or domino nor gate 310 for example.

When the circuitry illustrated in Figure 3 is simulated, it is necessary that each stage have each preceding stage fully simulated before that stage may be simulated. Thus if a current stage to be simulated is stage 375 then both stage 330 and stage 365 must have already been simulated. For that to happen, as will be appreciated, each preceding stage must have been simulated. Thus simulation of this circuit must begin with simulation of one of the four initial stages 305, 310, 340 or 345. Each of those stages may be thought of as a first stage. Once those stages are simulated then a second stage, such as stage 315 or 350, may be simulated. Once those stages are

simulated then third stage 320 may be simulated. Once that stage has been simulated then fourth stage 325 may be simulated. To simulate stage 330 both stage 325 and stage 360 must be simulated. Stages 350, 355 and 360 may be simulated as static circuitry.

Because stages 350, 355 and 360 (among other stages) are static circuitry they are not simulated in the same way as domino circuitry is. Rather, stage 350 is simulated with the worst-case output noise of stages 345 and 340 at a DC level rather than simulating the AC transition. That in turn results in the worst-case output noise for stage 350 which is simulated as the worst-case input noise for stage 355. Similarly, the worst-case output noise for stage 355 which is simulated as the worst-case input noise for stage 360. This results in a worst-case output noise for stage 360 which may be used as a level offset or level shift entered into stage 330 and also injected into stage 365. Stage 330 may then be simulated as may stage 365. When both stage 330 and stage 365 have been simulated then stage 375 may be the current stage and may be simulated.

Turning to Figure 4A, an embodiment of a method of simulating domino logic such as the domino circuitry of Figure 3 is illustrated. In block 400 the parameters of each domino circuit stage are extracted. These parameters include all of the information necessary to simulate the domino circuit stage. Also at block 400 the first stage, a stage with no prior domino circuitry feeding into it is found. That first stage is called the current stage. At block 410 a check is made to determine whether the current stage has any prior stages which need to be simulated. If all prior stages have been simulated the process flows to block 420 and the current stage is simulated

resulting in information on the worst-case noise that will be generated by the current stage. The process then flows to block 430 where it is determined whether any remaining stages have not been simulated. If no stages have not been simulated (all stages simulated) then the results of all of the simulations are reported including the indication of which circuitry blocks or stages appear likely to generate an erroneous output or input. This occurs at block 440. If any stages still need to be simulated the process flows to block 450 and the next unsimulated stage is listed as the current stage. The process then flows to block 410 where it is determined whether all stages prior to the current stage have been simulated. If not all stages prior to the current stage have been simulated in block 410 the process flows to block 460 and a prior stage of the current stage is made the new current stage. The process then flows back to block 410. At this point the process will either flow to block 420 or block 460 as appropriate and follow the same process that has already been outlined.

As a result, utilizing this process on circuitry illustrated in Figure 3, if stage 375 was the first stage to be simulated then the process would move back through the circuitry illustrated until it got to one of stages 305, 310, 340 or 345, it would then simulate up to either stage 315 or stage 350 after simulating at least two of the four initial stages. It would then simulate along the chain as far as it can get, typically up to stage 330 or 365. It would then have to back-propagate through the rest of the circuitry and simulate the other half of the circuitry illustrated in Figure 3. Once all of the stages leading up to stage 375 were simulated then stage 375 itself could be simulated. At that point there would no remaining unsimulated stages and a report of the results of the simulation could be made.

Turning to Figure 4B, an alternate embodiment of a method of simulating domino circuitry is illustrated. At block 470, all information about all domino circuits is extracted (such as extracting from a netlist or similar file containing design and/or layout information). The process then flows to block 475, where the order in which the domino and other stages should be simulated is determined such that each stage will be simulated after all preceding stages are simulated, thus guaranteeing that a stage may be simulated with information about all possible injected noise (based on the simulation). Block 475 may be implemented in part because netlists and other design files include information indicating how each signal is routed, and in part because distinguishing the inputs from the outputs of a circuit in a netlist or similar file can also be accomplished.

Proceeding to block 480, the first stage in the ordered list of stages produced at block 475 is simulated. The process then flows to block 490, where a determination is made as to whether any stages remain unsimulated. If some stages remain unsimulated, the process flows to block 485, and the next stage in the ordered list of stages produced at block 475 is simulated. If all stages have been simulated, the process flows to block 440, where the report of simulation results is generated. It will be appreciated that the report of results may be generated in the same manner whether the embodiment of Figure 4A or the embodiment of Figure 4B is used.

Applying the embodiment of Figure 4B to the schematic of Figure 3, a number of options for simulation of the domino circuitry may be found. For example, each of stages 305, 310, 340 and 345 may be simulated, after which stages 315 and 350 are simulated. (It will be appreciated that stages that are simulated in groups such as 305,

310, 340 and 345 may be simulated in series or parallel.) Following that, stages 320 and 355 are simulated. Next, stages 325 and 360 are simulated. Following that, stages 330 and 365 are simulated. Finally, stage 375 is simulated.

Alternatively, stages 305 and 310 may be simulated, followed by stage 315, then stage 320, then stage 325. Next, stages 340 and 345 may be simulated, followed by stage 350, then followed by stage 355, and then followed by stage 360. Then, stages 330 and 365 may be simulated. Finally, stage 375 may be simulated.

Turning to Figure 5, an embodiment of a method of designing a circuit utilizing, among other things, an embodiment of the method of simulating domino stages is illustrated. At block 500 the circuit is initially designed including a first pass design of all domino or static logic stages. At block 510 the domino stages and the entire circuit is automatically simulated. This results in a determination of which stages appear to be failing, that is appear to be generating or propagating noise which is outside of acceptable limits. The process then proceeds to block 520 where the failing stages are simulated in a customized manner by the designer to determine whether these failures are real or are in fact some sort of artifacts or inaccuracies of simulation. This custom simulation, in one embodiment, is implemented by the designer but it will be appreciated that to some degree this custom simulation may also be automated. The process then flows to block 530 where it is determined whether there are any real failures in the circuit. If there are real failures the process flows to block 550 where the designer redesigns the circuit to eliminate or reduce the noise encountered in the failing stages. The process then flows back to block 510 and the stages are simulated again. After the stages are simulated again the process flows to block 520, and another

custom simulation of any failing stages is performed. The process then flows to block 530. If no real failures are encountered then the design is believed to be complete and the process flows to completion block 540. Otherwise the process may loop around as many times as necessary until the circuit is believed to be passing the check for noise implemented in the simulation of stages.

Turning to Figure 6, an illustration of a machine readable medium embodying instructions suitable for execution by a processor, is illustrated. Medium 600 embodies instructions for circuit or node extraction 610 which when executed by a processor causes the processor to extract the parameters for the various stages previously discussed. Medium 600 also embodies simulation scheduler 620 which schedules which stage should be simulated next by determining whether that stage depends on any stages which have not yet been simulated. Medium 600 also embodies simulation software 630 which actually simulates each stage once simulation scheduler has determined which stage should be simulated next. Medium 600 also embodies master report generator 640 which takes the results of each invocation of simulation software 630 and compiles those results into a master report suitable for viewing or analysis by the designer.

Turning to Figure 7, a system suitable for implementation or execution of the method discussed previously is illustrated. The system includes processor 710 which is coupled to memory control hub 720. Memory control hub 720 is coupled to memory 730. Memory control hub 720 is also coupled to monitor interface 770 and memory control hub 720 is coupled to input/output hub 740. Monitor interface 770 is coupled to monitor 780. Input/output hub 740 is coupled to bus 750. Bus 750 is coupled to one or

more peripherals 760. The machine readable medium of Figure 6 may be a medium readable by one of peripherals 760. It may also be memory 730. A machine readable medium may be some form of memory such as random access or read only memory. It may also be a magnetic medium such as a tape or disk and may further be embodied in a carrier wave or other receivable medium, and may also be embodied in an optical medium. The machine readable medium will embody instructions which may be executed by processor 710 to cause processor 710 to extract information about each node of the circuit, schedule simulation of those nodes, simulate those nodes, and generate report information about those nodes. Report information may be stored in memory 730 or by one of peripherals 760 or may be displayed on monitor 780.

In the foregoing detailed description, the method and apparatus of the present invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the present invention. The present specification and figures are accordingly to be regarded as illustrative rather than restrictive.

CLAIMS

What is claimed is:

1. A method comprising:

extracting parameters of a set of domino logic circuits;

simulating each domino logic circuit of the set of domino logic circuits; and

reporting results of the simulating.

2. The method of claim 1 wherein:

each domino logic circuit having a set of inputs and an output and

simulating each domino logic circuit after any circuits coupled to the set of inputs have been simulated.

3. The method of claim 2 wherein:

simulating each domino logic circuit includes using the simulated results of circuits coupled to the inputs of the domino logic circuit.

4. A method comprising:

scheduling a set of domino logic circuits into an ordered list; and

simulating each domino logic circuit according to the ordered list.

5. The method of claim 4 further comprising:

extracting the parameters for each domino logic circuit of the set of domino logic circuits.

6. The method of claim 5 further comprising:

reporting results of the simulating.

7. The method of claim 6 wherein:

the scheduling includes scheduling the set of domino logic circuits such that all circuits coupled to an input of a first domino logic circuit are placed in the ordered list at a position in the ordered list before a position in the ordered list of the first domino logic circuit.

8. The method of claim 7 wherein:

the extracting further including extracting parameters of non-domino circuits;

the scheduling further including scheduling non-domino circuits into the ordered list; and

the simulating further including simulating non-domino circuits.

9. The method of claim 8 wherein:

the reporting further including reporting results of the simulating non-domino circuits.

10. A machine readable medium embodying instructions which, when executed by a processor, cause the processor to perform a method, the method comprising:

scheduling a set of domino logic circuits into an ordered list; and

simulating each domino logic circuit according to the ordered list.

11. The machine readable medium of claim 10 further embodying instructions which, when executed by a processor, cause the processor to perform the method further comprising:

extracting the parameters for each domino logic circuit of the set of domino logic circuits.

12. The machine readable medium of claim 11 further embodying instructions which, when executed by a processor, cause the processor to perform the method further comprising:

reporting results of the simulating.

13. The machine readable medium of claim 12 further embodying instructions which, when executed by a processor, cause the processor to perform the method wherein:

the scheduling includes scheduling the set of domino logic circuits such that all circuits coupled to an input of a first domino logic circuit are placed in the ordered list at a position in the ordered list before a position in the ordered list of the first domino logic circuit.

14. The machine readable medium of claim 13 further embodying instructions which, when executed by a processor, cause the processor to perform the method wherein:

the extracting further including extracting parameters of non-domino circuits;

the scheduling further including scheduling non-domino circuits into the ordered list; and

the simulating further including simulating non-domino circuits.

15. A system comprising:

a processor;

a memory controller coupled to the processor;

a memory coupled to the memory controller;

wherein the processor executes instructions to perform the method of:

scheduling a set of domino logic circuits into an ordered list; and

simulating each domino logic circuit according to the ordered list.

16. The system of claim 15 wherein the processor further executes instructions to perform the method further comprising:

extracting the parameters for each domino logic circuit of the set of domino logic circuits; and

reporting results of the simulating.

17. An apparatus comprising:

means for extracting parameters for each domino logic circuit of a set of domino logic circuits;

means for scheduling the set of domino logic circuits into an ordered list;

means for simulating each domino logic circuit according to the ordered list

means for reporting results of the means for simulating.

ABSTRACT OF THE DISCLOSURE

In one embodiment, the invention is a method. The method includes extracting parameters of a set of domino logic circuits. The method also includes simulating each domino logic circuit of the set of domino logic circuits. Also, the method includes reporting results of the simulation.

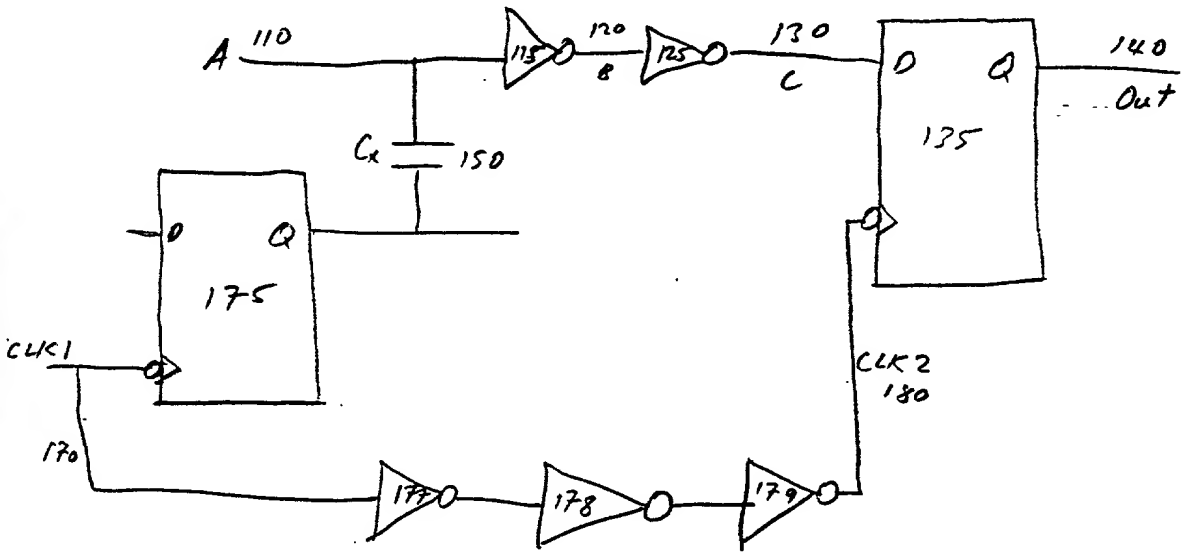

Fig. 1A

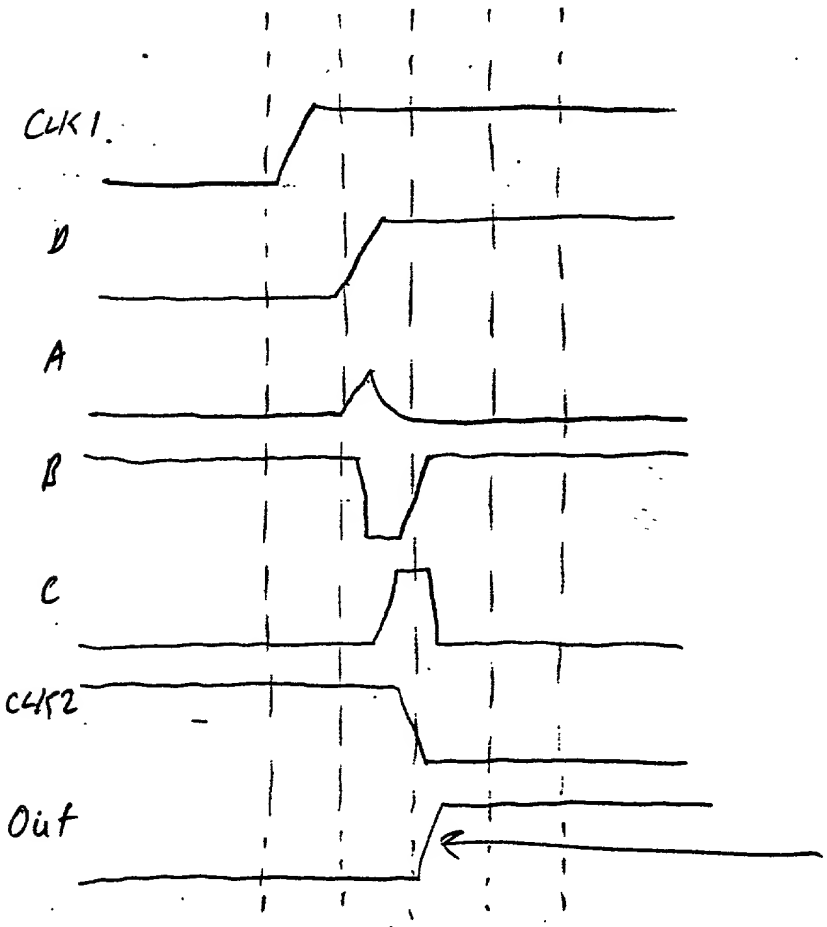

Fig. 1B

Fig. 2

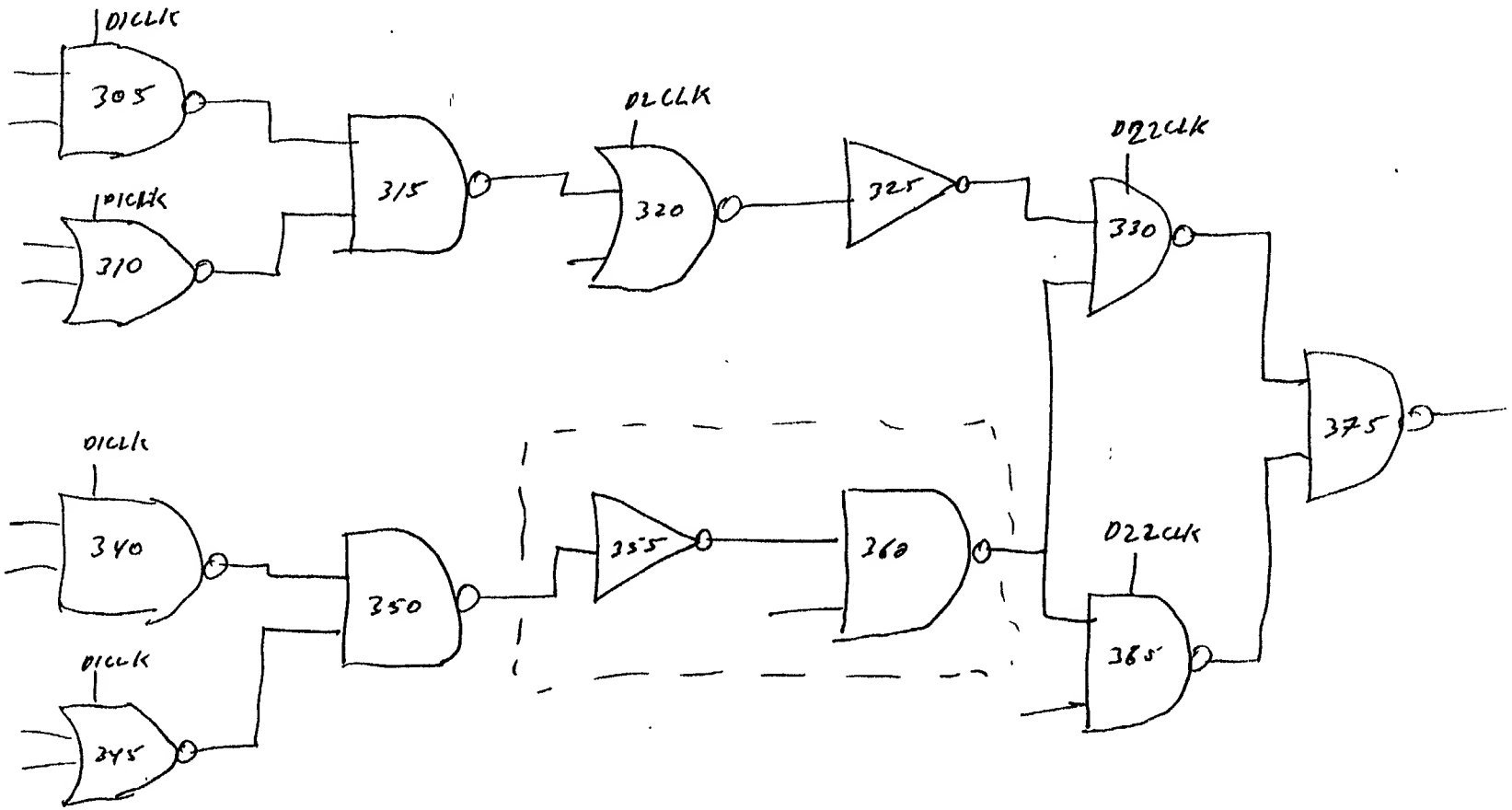

Fig. 3

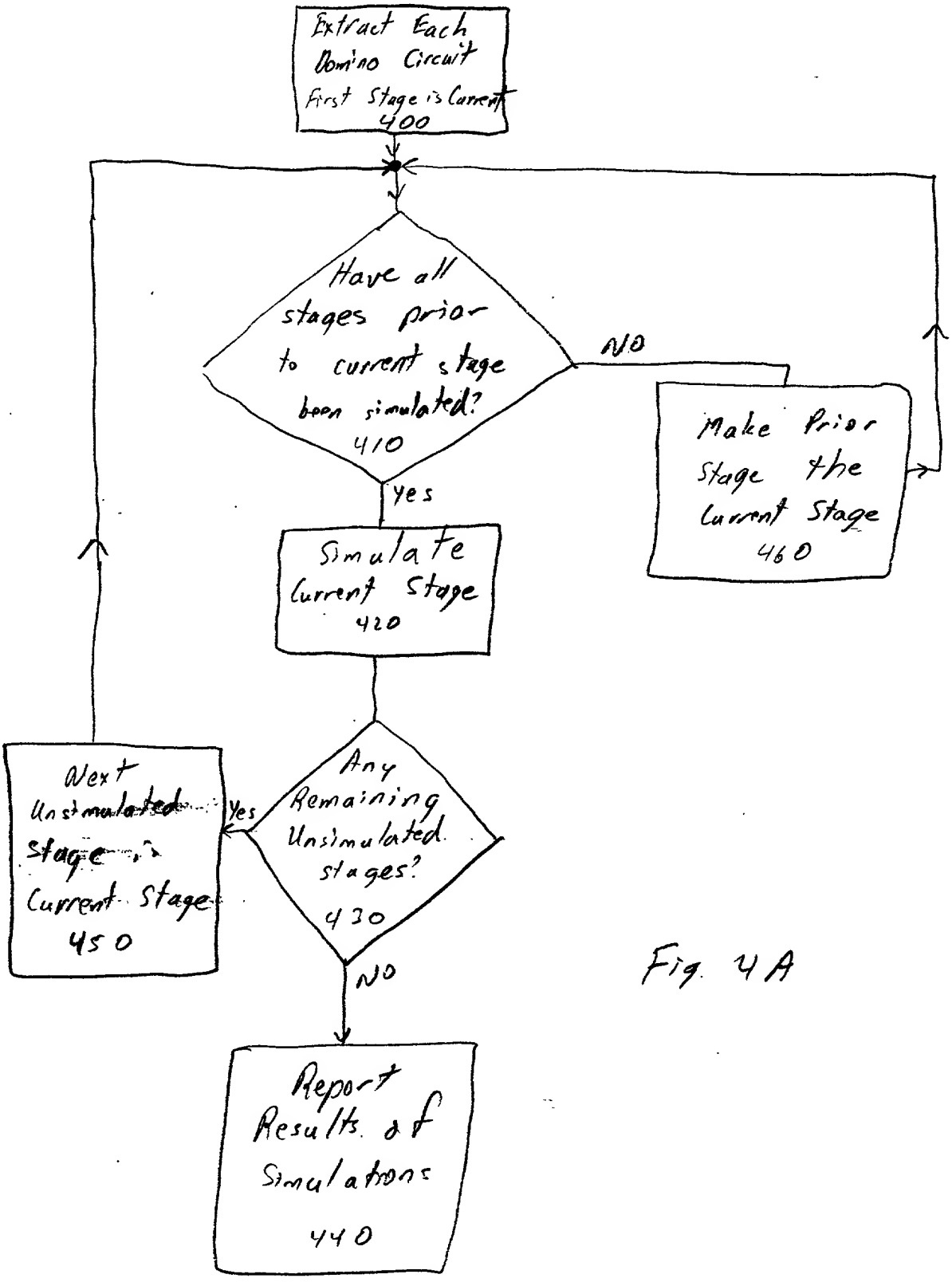

Fig. 4A

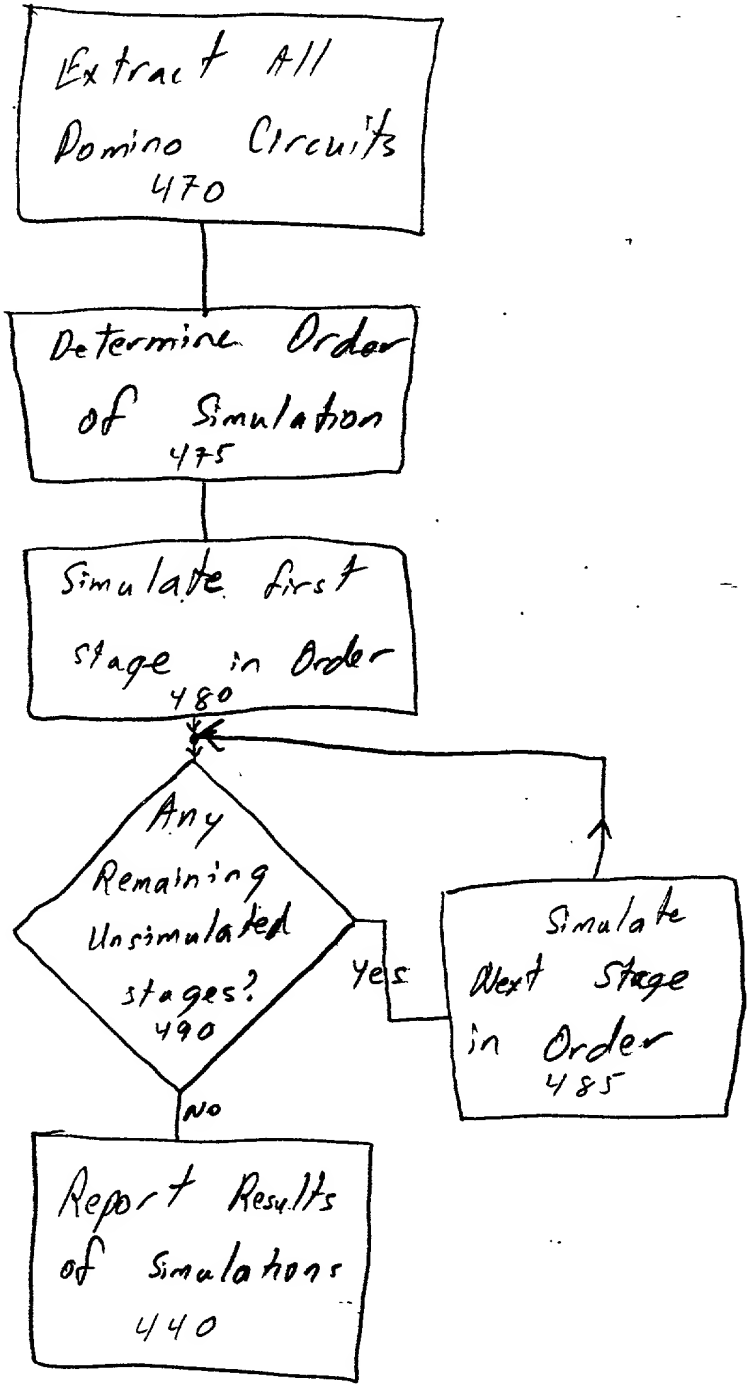

Fig. 4B

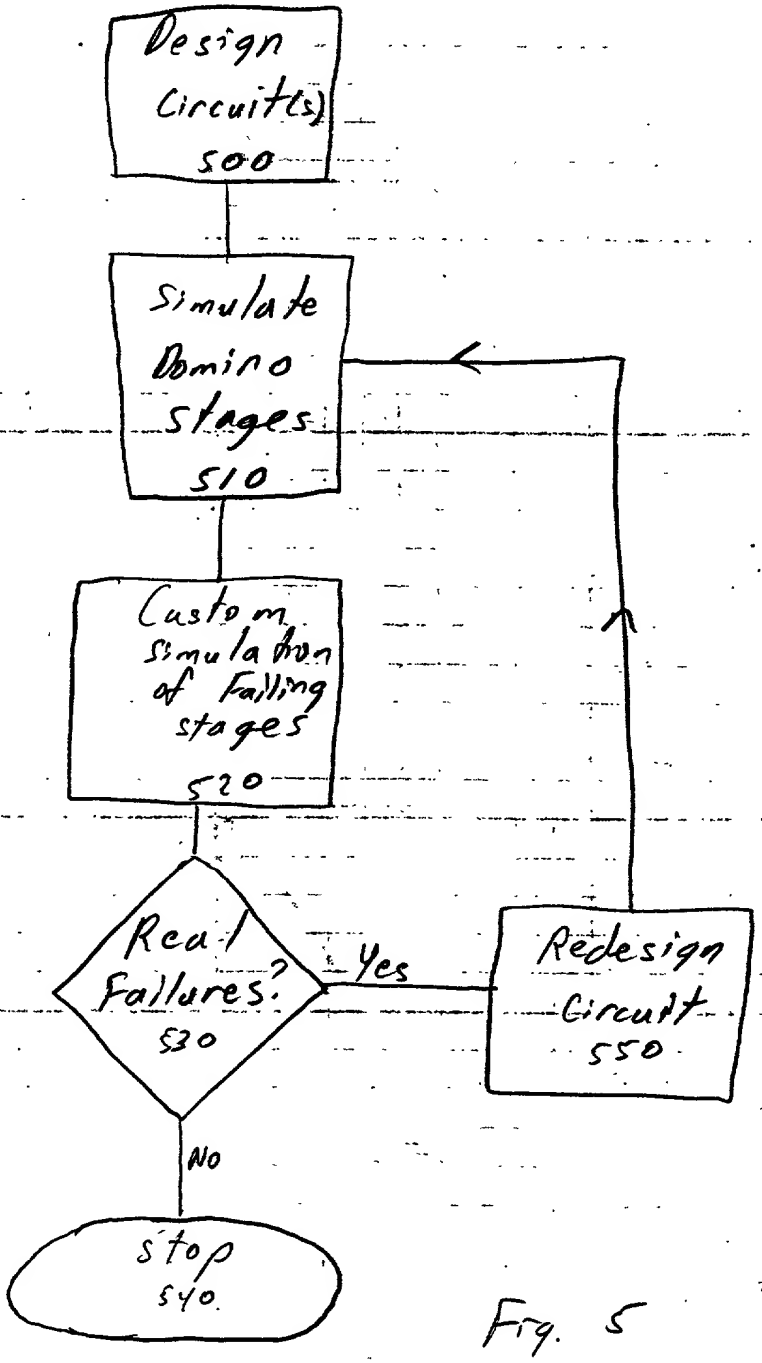

Fig. 5

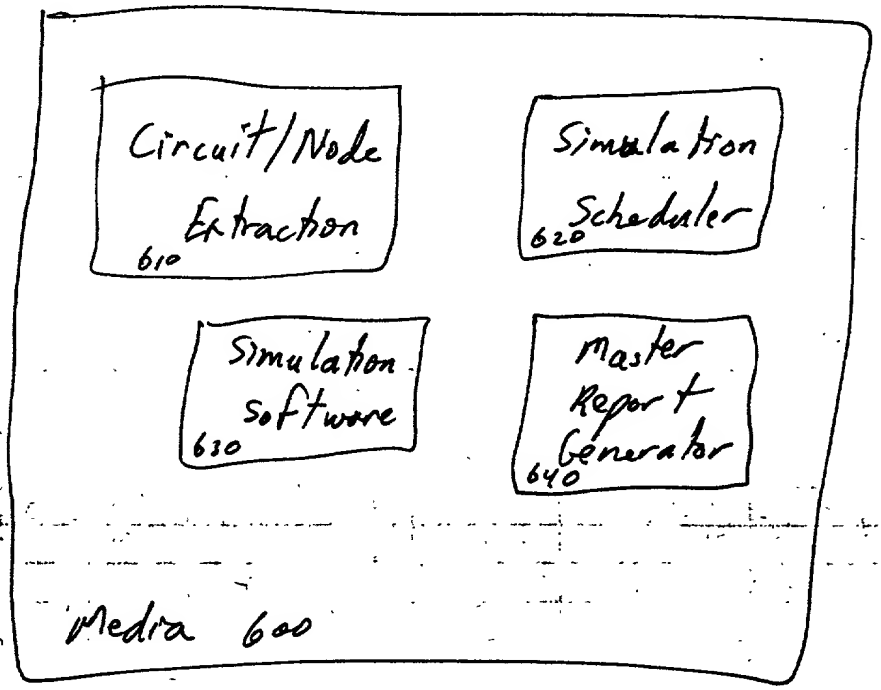

Fig. 6

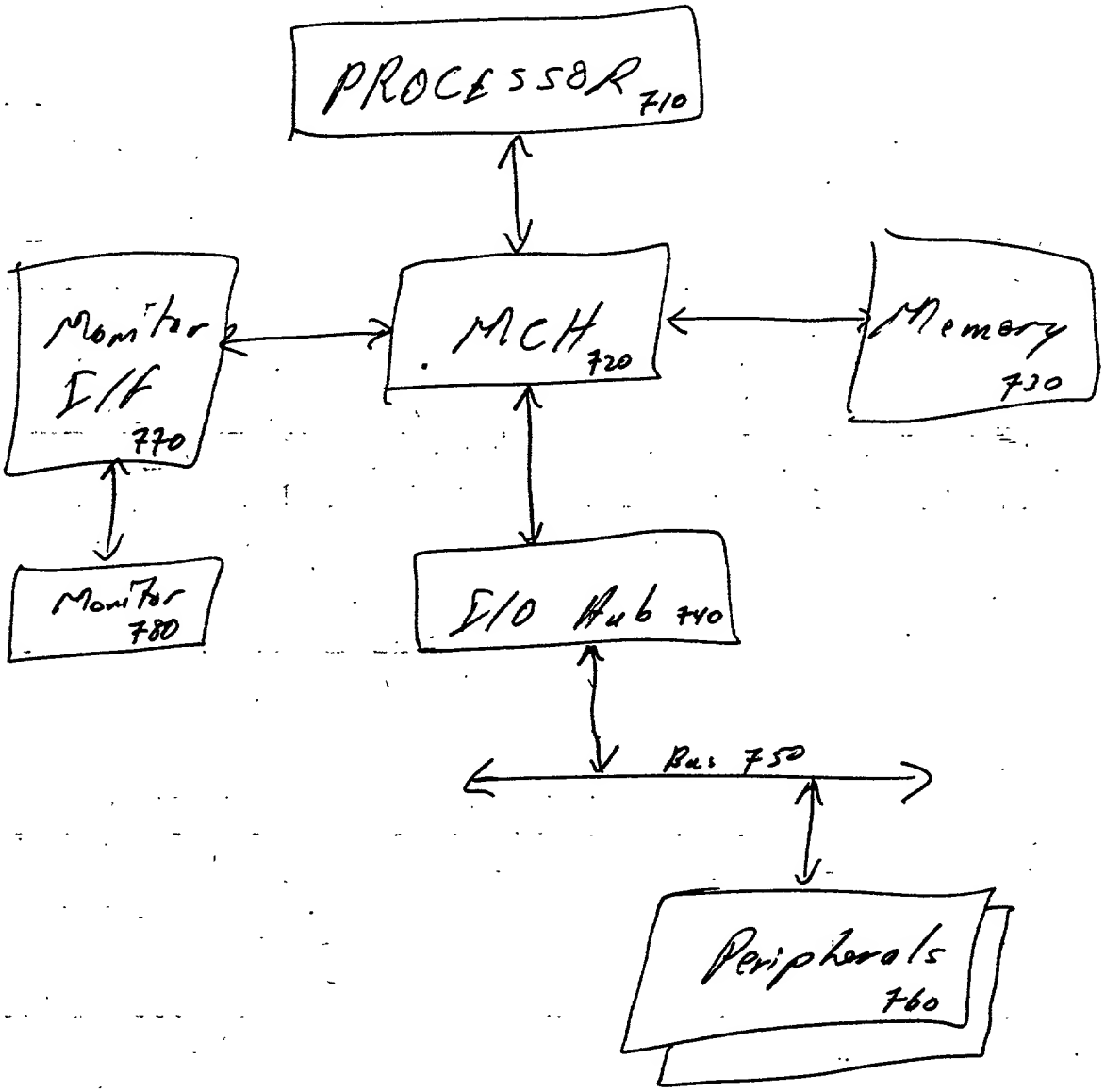

Fig. 7

Attorney's Docket No.: 042390.P6942 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
METHOD AND APPARATUS FOR FULLY AUTOMATED SIGNAL INTEGRITY ANALYSIS FOR DOMINO CIRCUITRY

the specification of which

_X_ is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)

(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned
Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Glenn E. Von Tersch, BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to Glenn E. Von Tersch, (408) 720-8598.
(Name of Attorney or Agent)
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Mark D. Nardin

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____

Full Name of Second/Joint Inventor Hans Greub

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____

Full Name of Third/Joint Inventor Sapumal Wijeratne

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State) (Country)

Post Office Address _____

APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.